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May 11 2006

Current DAQ Status and Rate Limitations

TDC Readout (COT)

Improved DSP processing
Optimized readout, using SPY mode
Changed data format to reduce data volume
Set maximum number of hits to 4/channel
Use Fast Clear to reduce DSP processing

CLC Readout

Added second TDC in crate

Using faster Front End Processors

MVME 5500 used in crates that require significant processing (PCAL)

Use Readout List

Control readout of diagnostic information (usually slow to read-out)

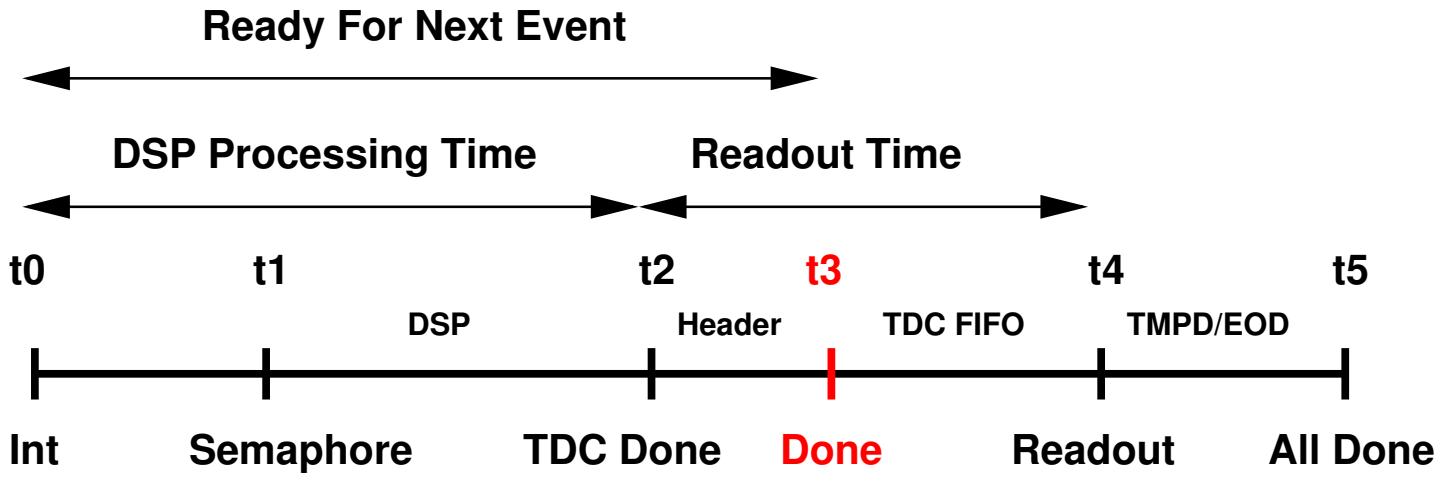
Expanded the number of VRB crates

DAQ VRB crates increased from 6 to 12.

Will be difficult to improve readout times beyond this...

All this was completed before we ran into problems...

Measuring Readout Times



Maximum of "Time to set TRACER done" and readout sets the overall readout rate

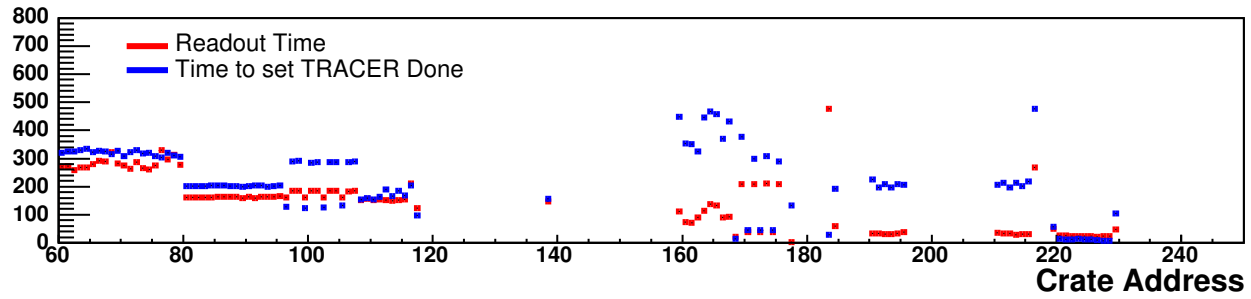
TMPD diagnostic bank stores the timing information

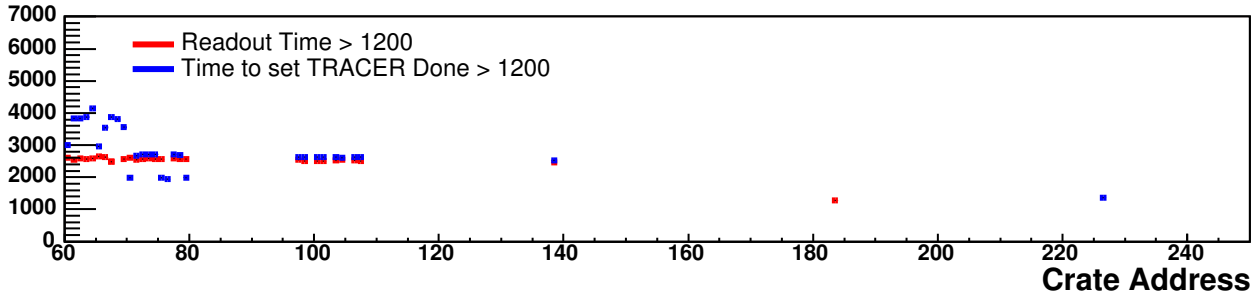
Front End sets the TRACER done (TS can issue next trigger).

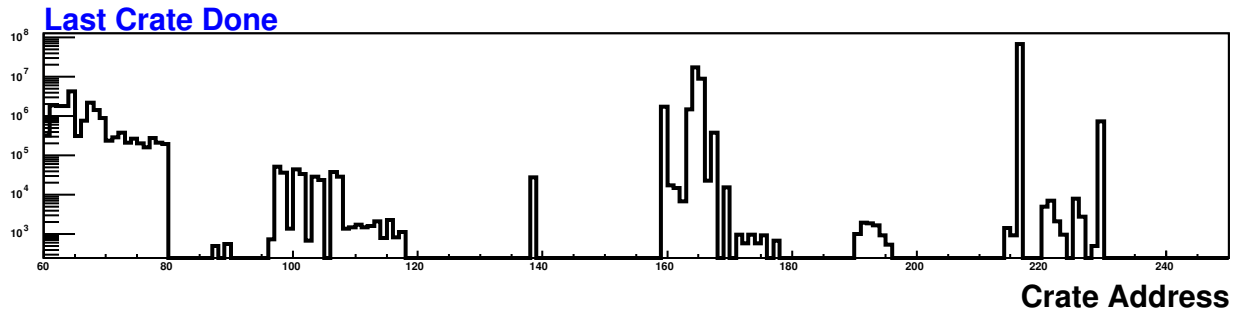
Readout/Reformatting is done after setting the TRACER done.

FE cards can process the next event while the current event is being readout

Which Crates are the Slowest?

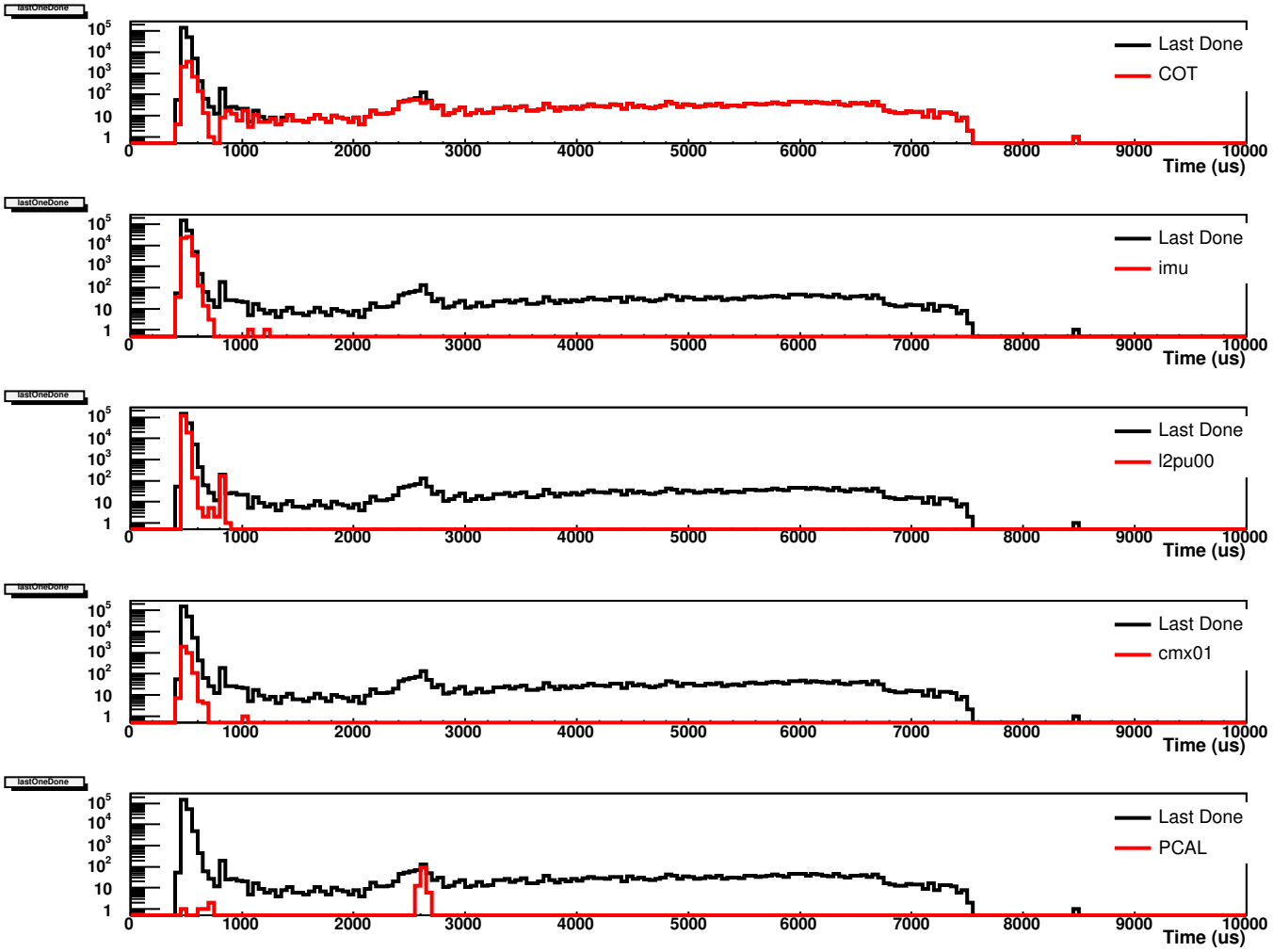






Mostly COT, IMU, l2pu00, PCAL...

Compares the time of the last crate done to specific crates (TDCs, IMU, l2pul00, cmx, PCAL)

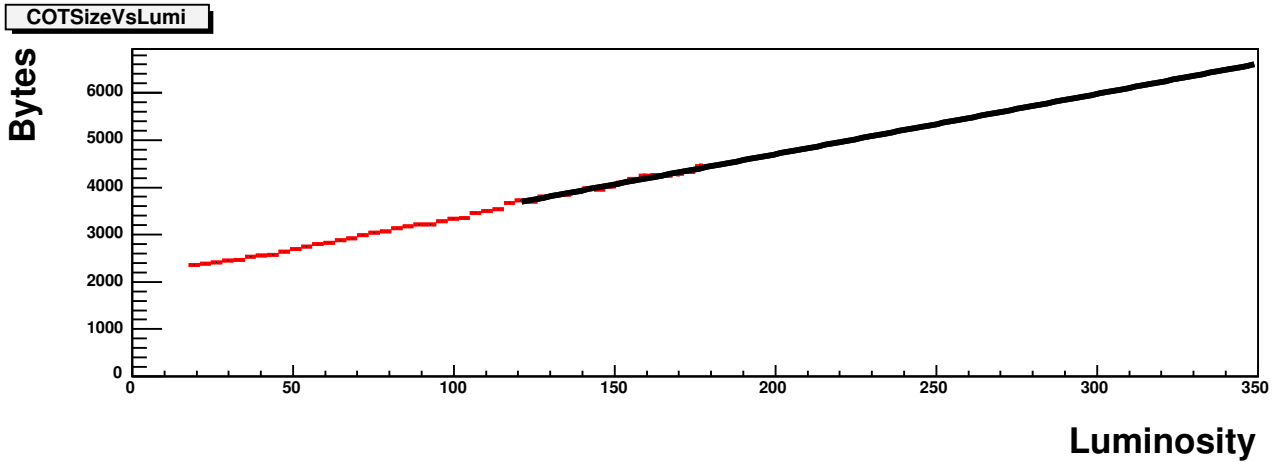


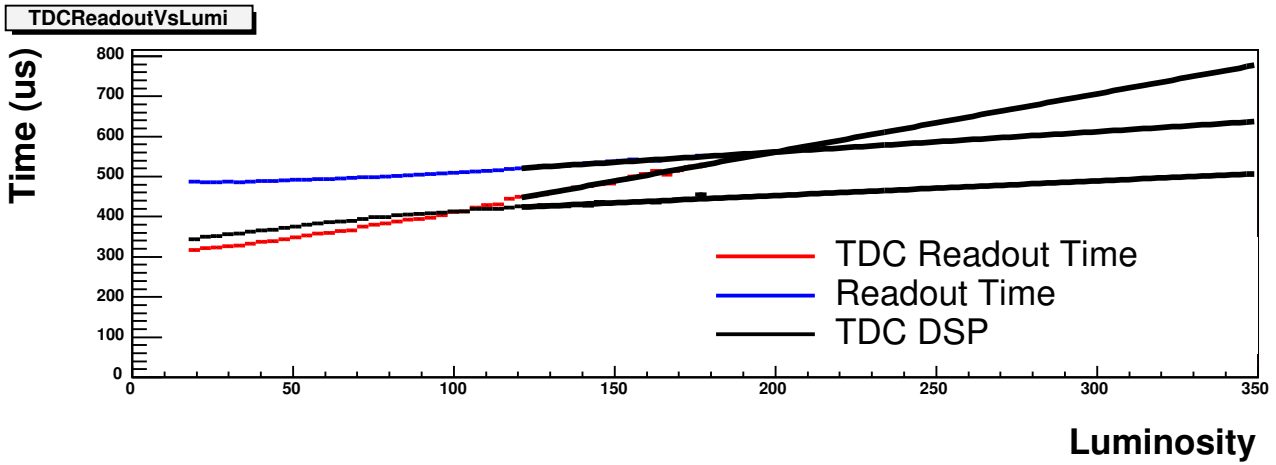
→ Can see long tails in the COT readout...

Effect of staging in the modification for fast clear?

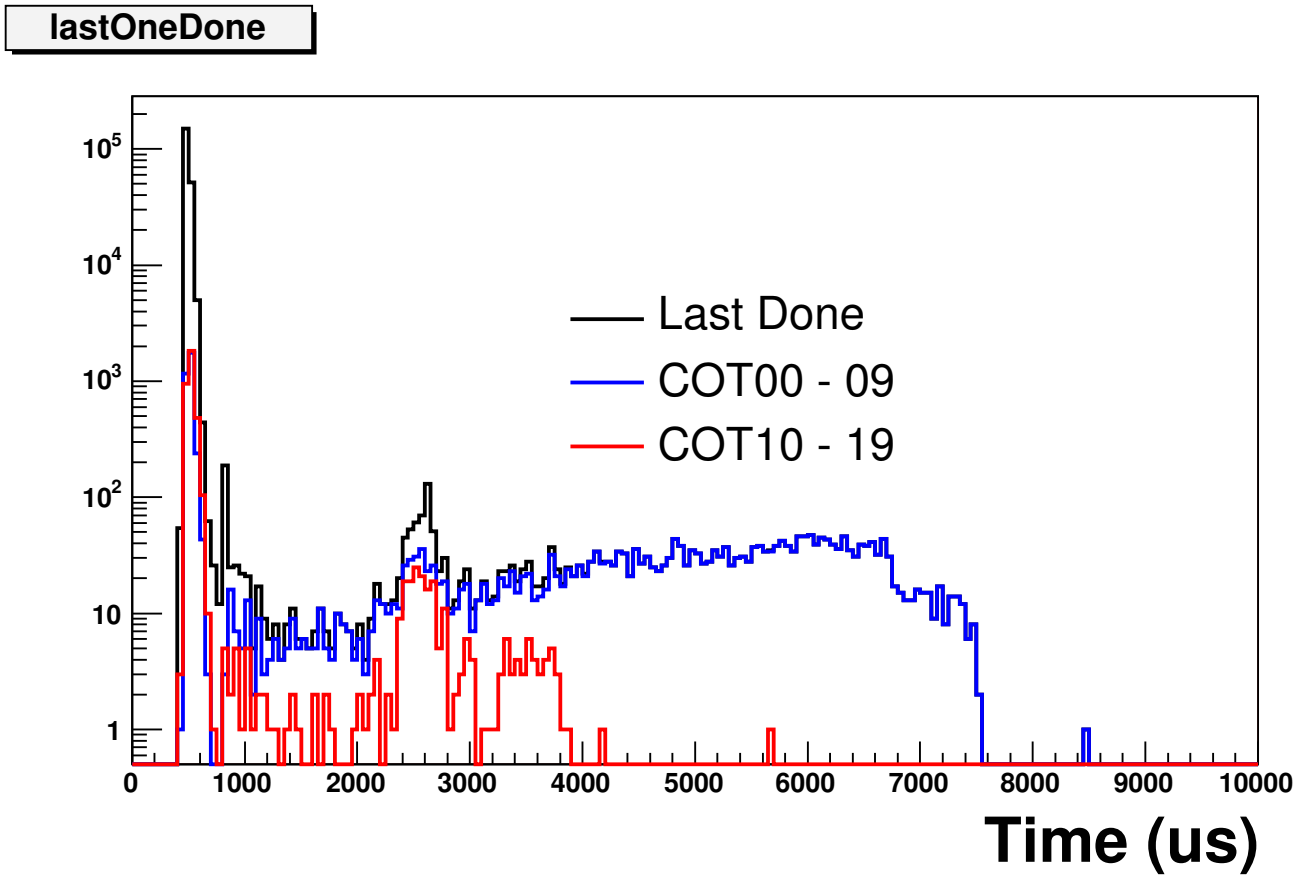
The increase in readout time with increasing luminosity looks reasonable

Expect that the COT readout will become the limiting factor... depends on the beam conditions/trigger mix





Some features in the readout will have to be understood...

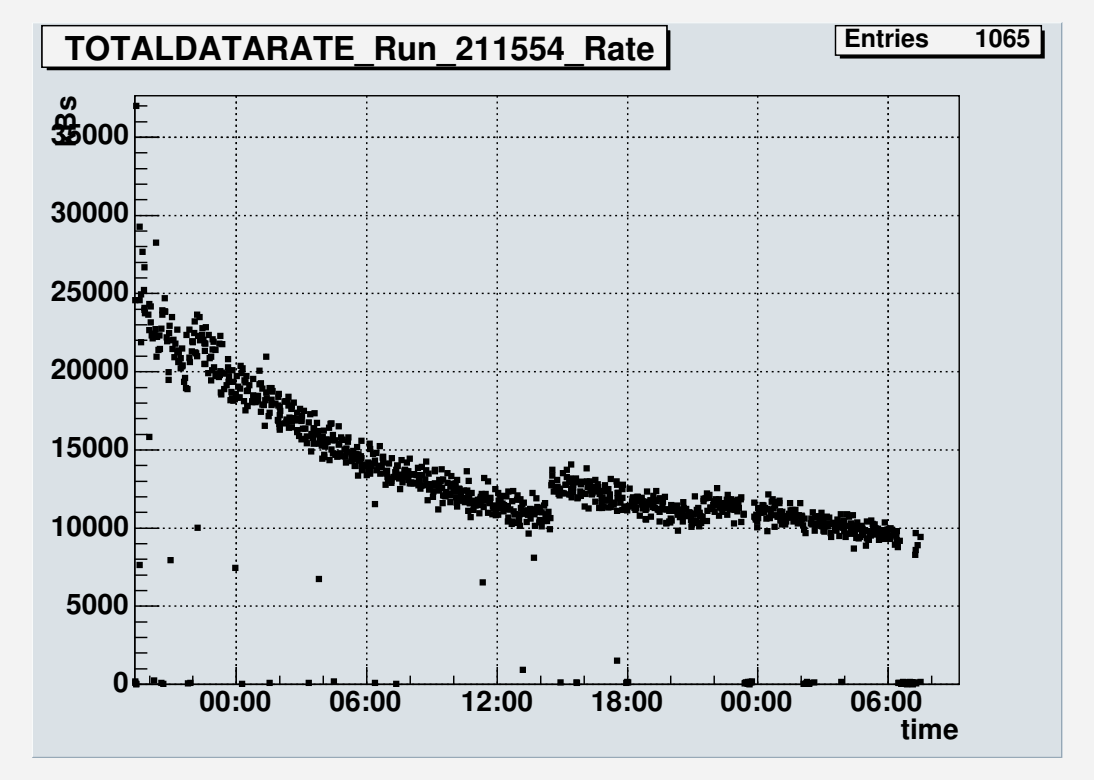


Long tails mainly coming from COT00-09

Why is there a cluster of events having long readout times for the PCAL crates...

CSL Upgrade

Run 211554 (2006.02.12)



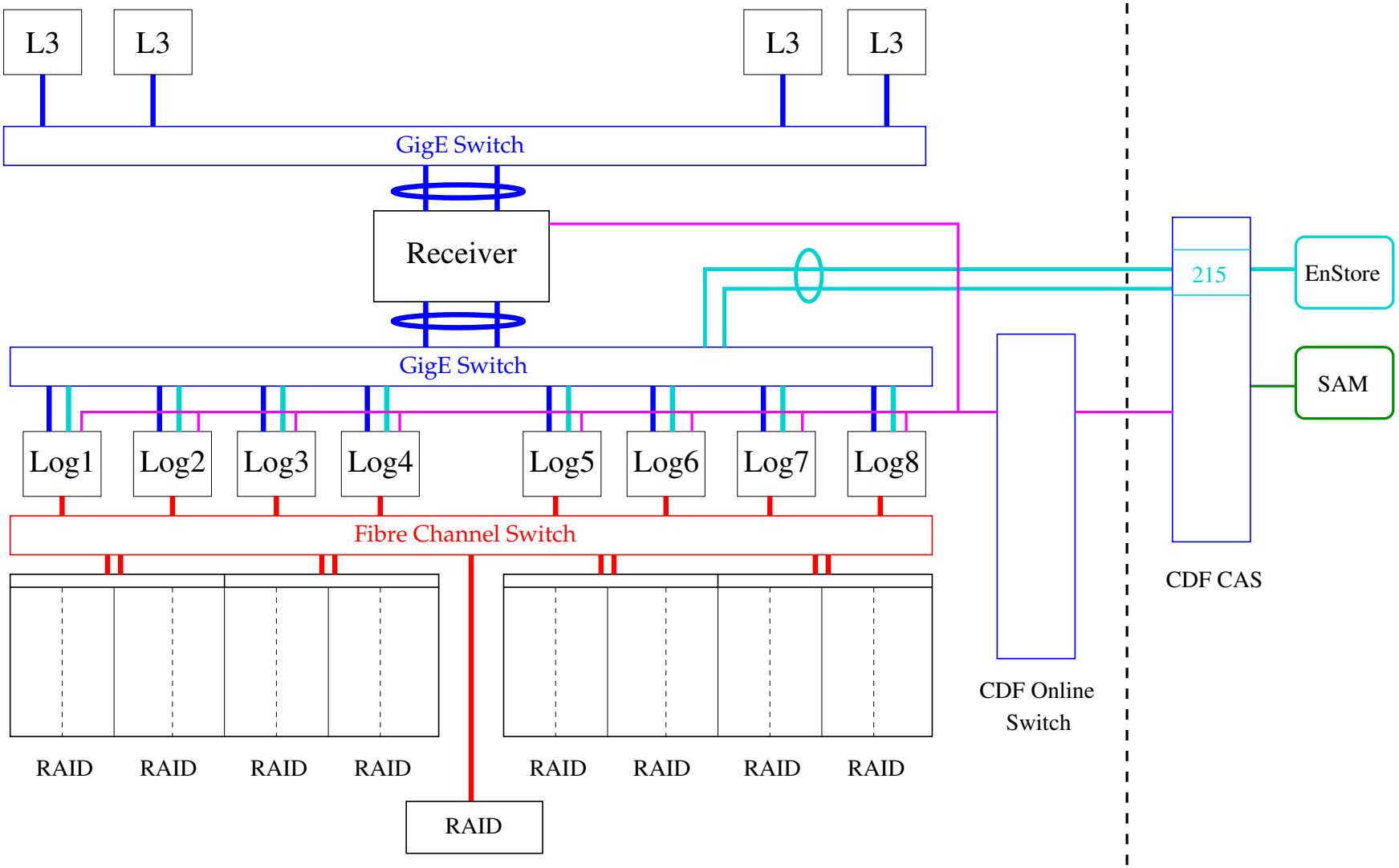
Current CSL limited to about 24 MB/s

What logging rate will we need?

250 KB/Event
1000 Hz
L3 rejection of 4-5 times
$\longrightarrow$ 50 - 63 MB/s

For high luminosity stores we are currently approaching the logging rate limit.

Can write to buffer disks at higher rates (45 MB/s) but cannot send data to Feynman fast enough (write to tape)



CSL upgrade should handle $\sim$ 80 MB/s

Using commodity hardware running Linux

Increased disk buffering capacity in BØ 4 $\rightarrow$ 20 TB

CSL Upgrade Status

Used prototype system to benchmark performance

Setup system for software development

Have successfully sent data from "L3 Sender" to receiver to Logger node.

Have written data from BØ to Feynman

All major equipment has been ordered and has arrived

Currently installing it into racks

Summary

Have made several significant improvements that reduce the read-out time $\rightarrow$ *Will be challenging to improve it any further*

Features in the readout times need to be understood

Need to watch for the impact of adding new banks...

Confident that we will be able to achieve the 1000 Hz goal.

Ultimately limited by TDC readout *(depends on occupancy)*

From Eric James' study...

- High luminosity/high occupancy

4 hits/ch on SL 1-4 (worst case scenerio...)
L1A 948 Hz $\rightarrow$ L2A 880 Hz 6% deadtime

- Low luminosity/low occupancy

Can achieve rates $>$ 1000 Hz